AN-732A
Application Note

A NON-VOLATILE MICROPROCESSOR MEMORY USING 4K N-CHANNEL MOS RAMS

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NMOS semiconductor technology has made inroads into high density/high performance circuit design. The one-chip microprocessor, Random Access Memories, and Read Only Memories, are changing system implementation from random logic designs to software and firmware programmable microcomputing systems. Such systems frequently require relatively large amounts of memory.

This paper describes the design of an 8192-byte non-volatile Random Access Memory system using the MCM6605A 4K x 1 RAM. The system is designed to work with the Motorola MC6800, an 8-bit microprocessor.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

Most read/write semiconductor memories are volatile, i.e., if power is removed from the memory the stored information will be lost. In many cases of power failure, non-volatility for a specific period of time is required either as a necessity (irreplaceable information) or as a convenience (to avoid reloading the memory).

This paper describes the design of an 8192-byte non-volatile memory system using dynamic RAMs and CMOS control logic in order to significantly reduce the power requirement in the standby mode of operation with respect to the normal operating mode.

This system was designed to be an add-on memory for the EXORciser,* a system development tool in the M6800 Microcomputer family.

MEMORY DEVICE DESCRIPTION

The memory device used in this system is the MCM6605A, a 4096-word x 1-bit dynamic Random Access Memory (RAM). The dynamic characteristic of this memory device requires that refreshing of the memory cells be performed at periodic intervals in order to retain the stored data. This device was chosen for the following features: high bit density per chip and correspondingly low price per bit, standby mode with low power dissipation, TTL compatibility of inputs and outputs, and speed characteristics compatible with microprocessors and the EXORciser.

Figure 1 is a functional block diagram of the MCM-6605A. The device uses a three-transistor storage cell in an inverting cell configuration. The single external high-level Chip Enable clock starts an internal three-phase clock generator which controls data handling and routing on the memory chip. The lower 5 address lines (A0 to A4) control the decoding of the 32 columns, and the upper 7 address lines control the decoding of the 128 rows within the memory chip. The Chip Select ($\overline{CS}$) input is used for memory expansion and controls the I/O buffers: when $\overline{CS}$ is low the data input and output are connected to the memory data cells, and when $\overline{CS}$ is high the data input is disconnected and the data output is in the high impedance state. Refreshing is required every 2 ms and is accomplished by performing a write cycle with $\overline{CS}$ high on all 32 columns selected by A0 through A4. The read/write line controls the generation of the internal $\phi 3$ signal which transfers data from the bit sense lines into storage.

All inputs and outputs with the exception of the high-level Chip Enable signal are TTL compatible, and the outputs feature three-state operation to facilitate wired-OR operation. The Chip Enable signal has ground and +12 V logic levels. Power requirements are typically 330 mW per device in the active mode from +12 V, +5 V, and -5 V power supplies, and 2.6 mW in standby with refresh from the +12 V and -5 V power supplies (the +5 V supply powers the output buffers and is not required during standby operation).

Memory timing is outlined in Figure 2 and operates as follows for a read cycle (Figure 2a). The Chip Enable line is brought high after the correct addresses are set up, which starts the internal three-phase clock and latches the addresses into an internal register. Chip Select must be brought low in order to connect the data input and output to the data cells, and the Read/Write line must be brought high to inhibit the $\phi 3$ cycle which writes data into the storage cells. A write cycle (Figure 2b) occurs in exactly the same manner as a read cycle except that the R/W line is placed in the Write mode, which gates the input data onto the bit sense lines, and enables a $\phi 3$ cycle to write into the data cells. A write and a refresh cycle are the same with the exception of Chip Select, which is held high for a refresh cycle and low for a write cycle.

The Read-Modify-Write cycle shown in Figure 2c is a read followed by a write within the same CE cycle. $\overline{CS}$ is brought low shortly after the leading edge of CE and R/W is held high long enough for the Data Out to become valid. The R/W line can then be strobed low for a minimum write time to enter the Data In (which has been placed on the input) into the data cells.

By holding the Chip Select high during refresh, the input data is inhibited from modifying the bit sense lines and the original data is returned to the data cells during $\phi 3$ of the cycle. This refreshing action recharges the storage cells and must be done at least every 2 ms if the memory is to retain the information. The fact that the data is stored on a capacitor in a dynamic memory (rather than the "On" transistor of a static memory) requires that the capacitor be recharged periodically. This capacitive storage produces a low power standby mode of operation where only refreshing takes place, which is the foundation of this low current drain non-volatile memory design. The memory

*Trademark of Motorola Inc.

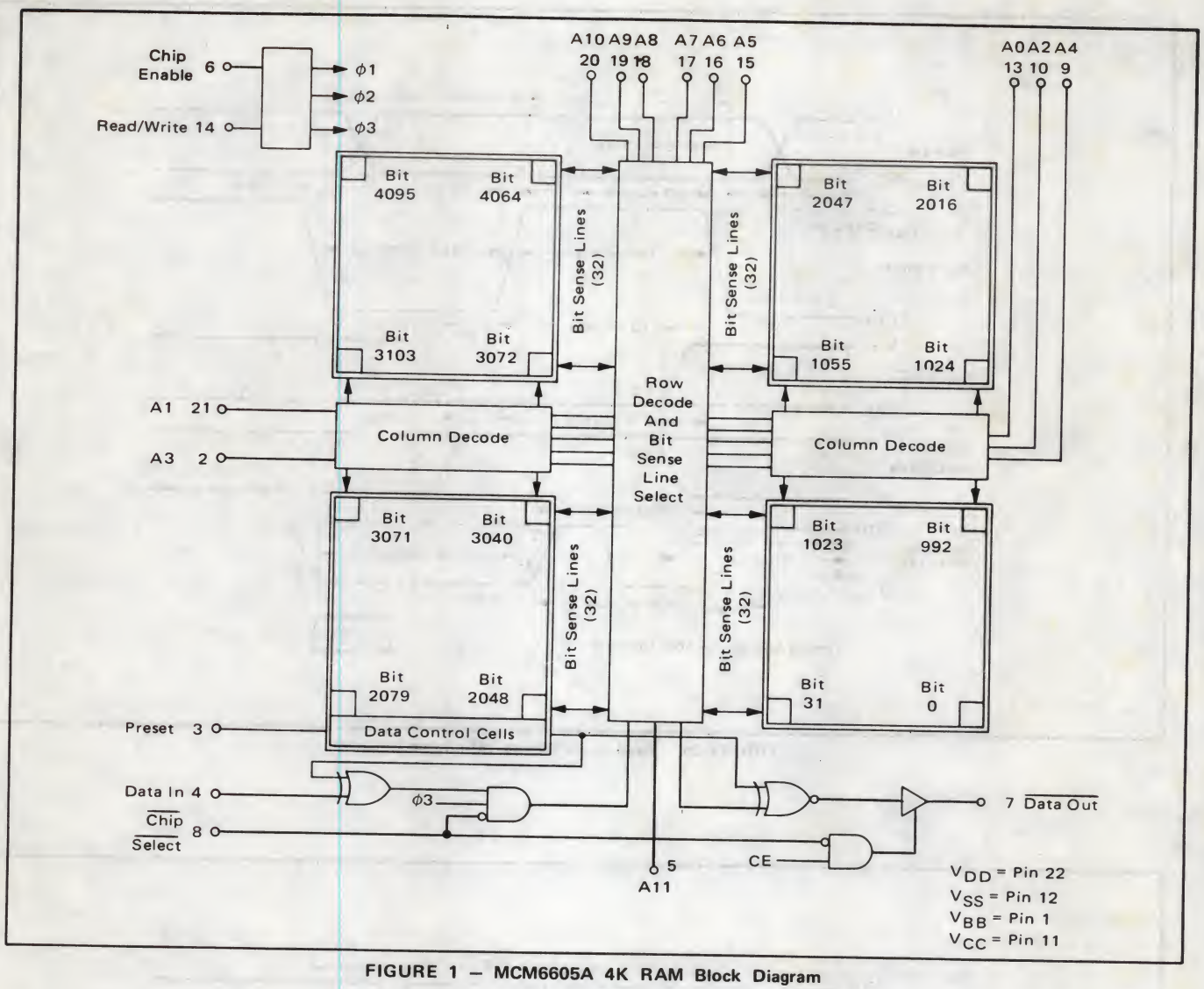

FIGURE 1 – MCM6605A 4K RAM Block Diagram

device typically dissipates 330 mW in the active mode but only 2.6 mW in the standby mode (refreshing only).

MEMORY SYSTEM DESIGN REQUIREMENTS

This memory system was designed with the following major design goals:

First, non-volatility for a period of time in the range of 7 to 10 days from a reasonably sized battery. It is also desirable for the system to operate from one battery voltage during the standby mode to simplify the battery requirements. Second, the memory size was desired to be 8K bytes on a PC card easily expandable upward and addressable in 4K byte blocks. Third, the memory system must be able to interface with the MC6800 microprocessor which has a basic cycle time of 1 μs. Fourth, the memory system controller must handle all refresh requirements in a manner as invisible as possible to microprocessor operation.

MEMORY SYSTEM DESCRIPTION

A block diagram of the memory system is detailed in Figure 3. This block diagram can be split into three main sections as follows. The first section is comprised of the address buffers, Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering and the memory array itself. The memory array consists of sixteen memory devices (4K words x 1-bit) organized into two rows of 4096 bytes each. The third section of the block diagram comprises the refresh and control logic for the memory system. This logic handles the timing of the refresh handshaking with the EXORciser to request a refresh cycle, the generation of the refresh addresses, synchronization of the $\overline{\text{Power Fail}}$ signal, multiplexing of the external Memory Clock with the internal clock (used during standby), and generation of the -5 V supply on the board by a charge pump method.

Figure 4 is a worst case timing diagram of the read and write cycles of the EXORciser and the 4K memory system. The timing is composed of two phases. During phase 1 (ϕ1) addresses are set up and during phase 2 (ϕ2) data is transferred. Figure 5 is a timing diagram of the memory system in standby showing refresh cycles only. This timing analysis will be referred to in the following discussions of the memory control circuitry.

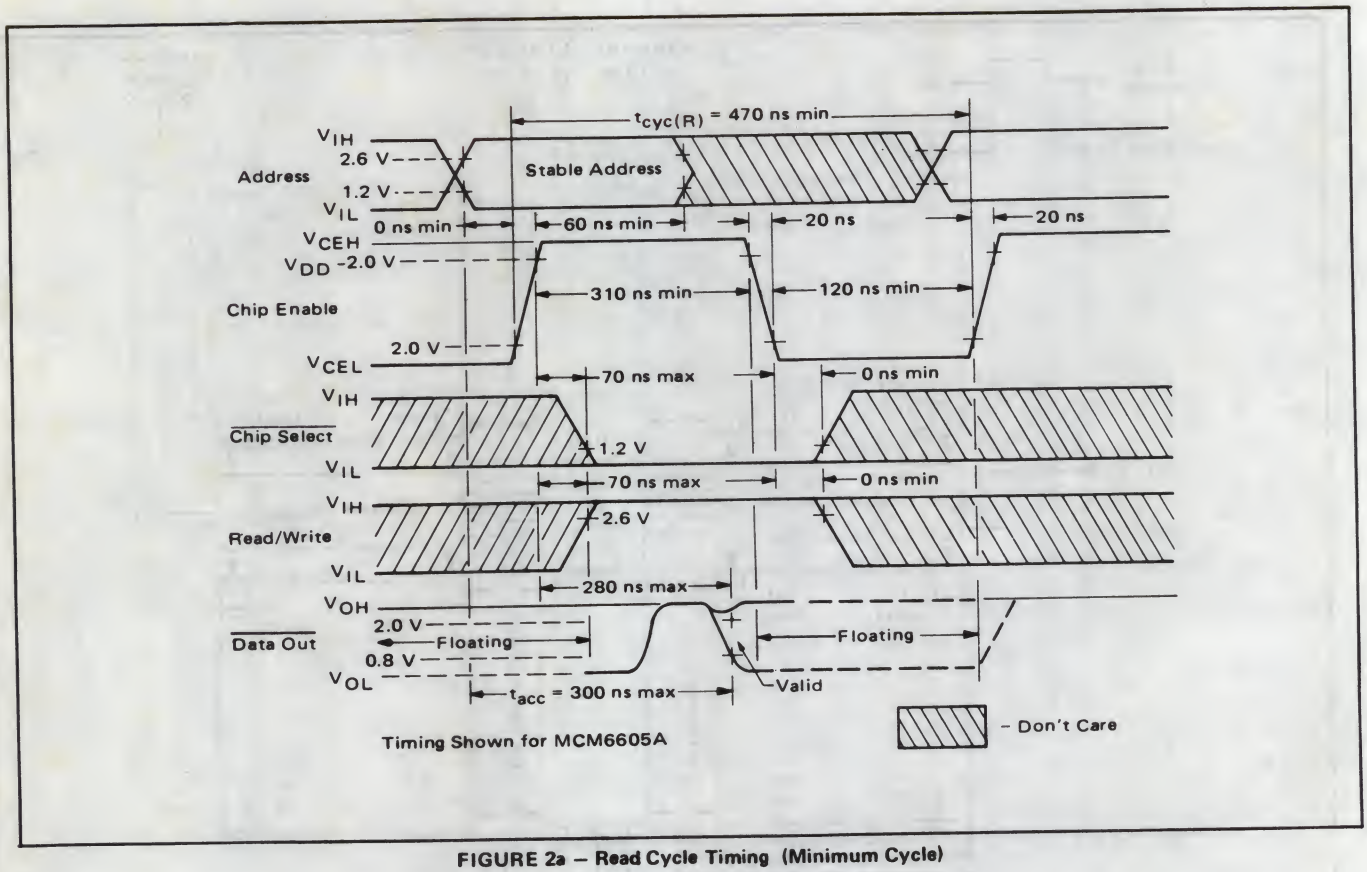

FIGURE 2a – Read Cycle Timing (Minimum Cycle)

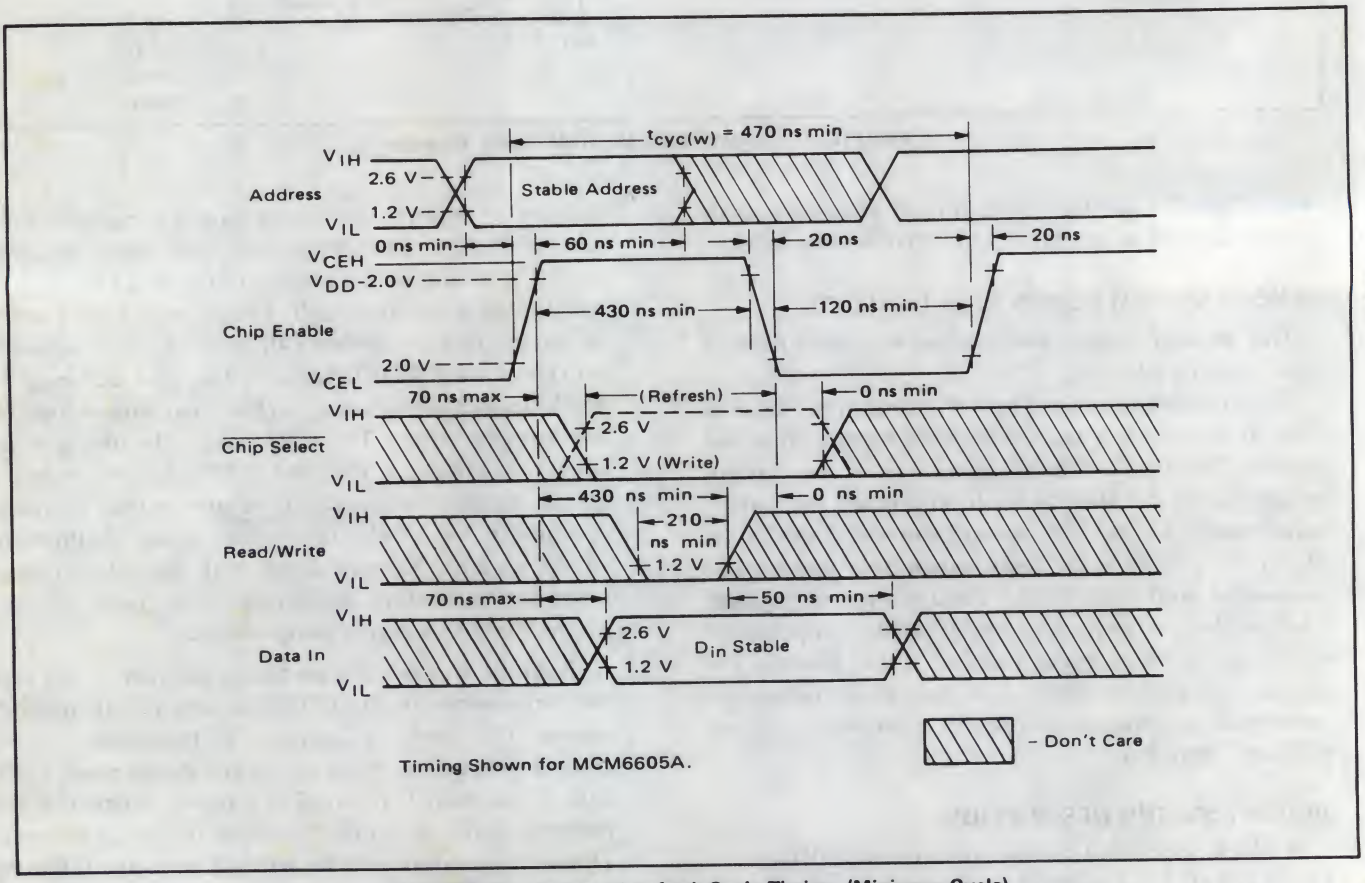

FIGURE 2b – Write and Refresh Cycle Timing (Minimum Cycle)

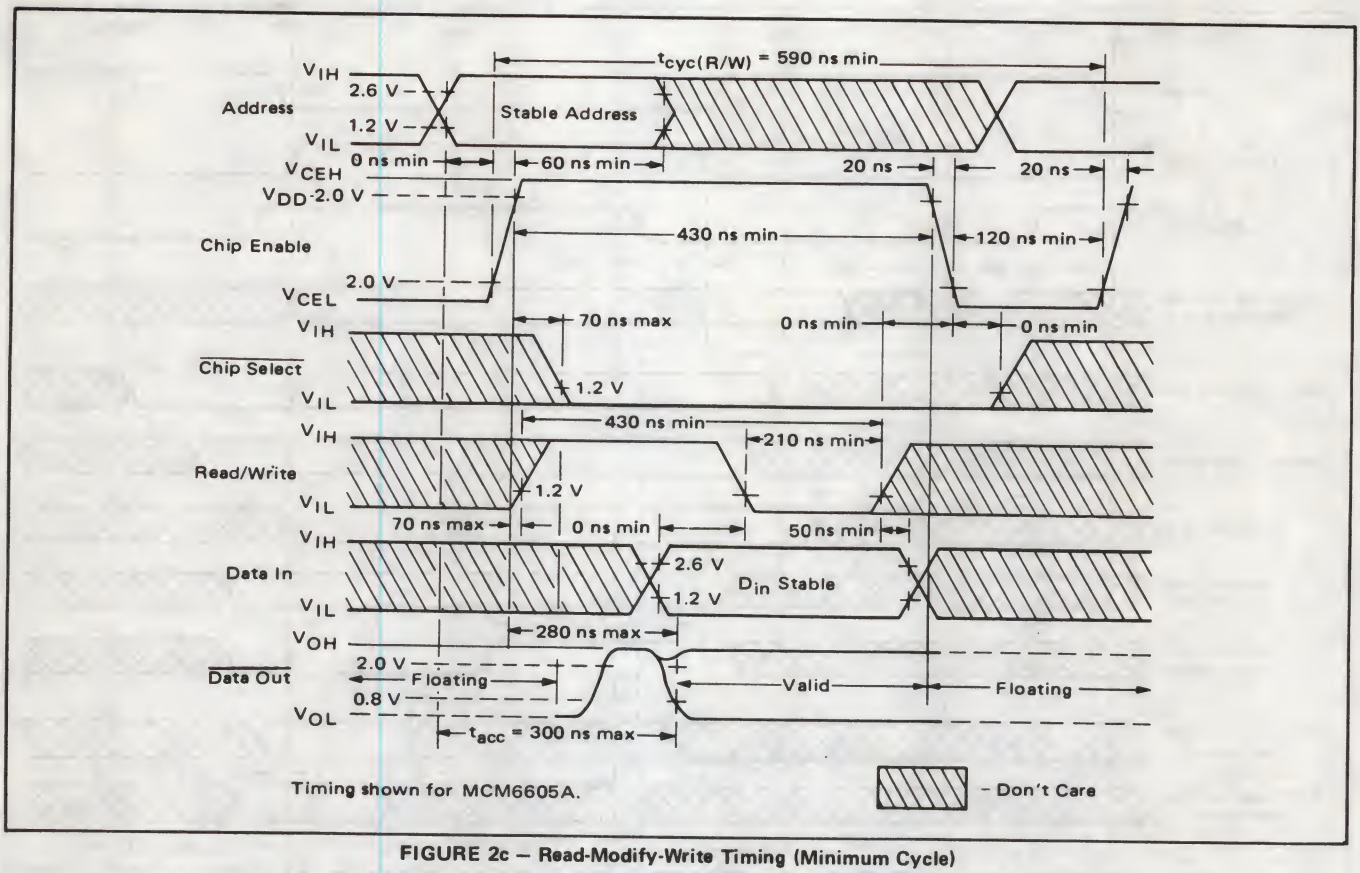

FIGURE 2c – Read-Modify-Write Timing (Minimum Cycle)

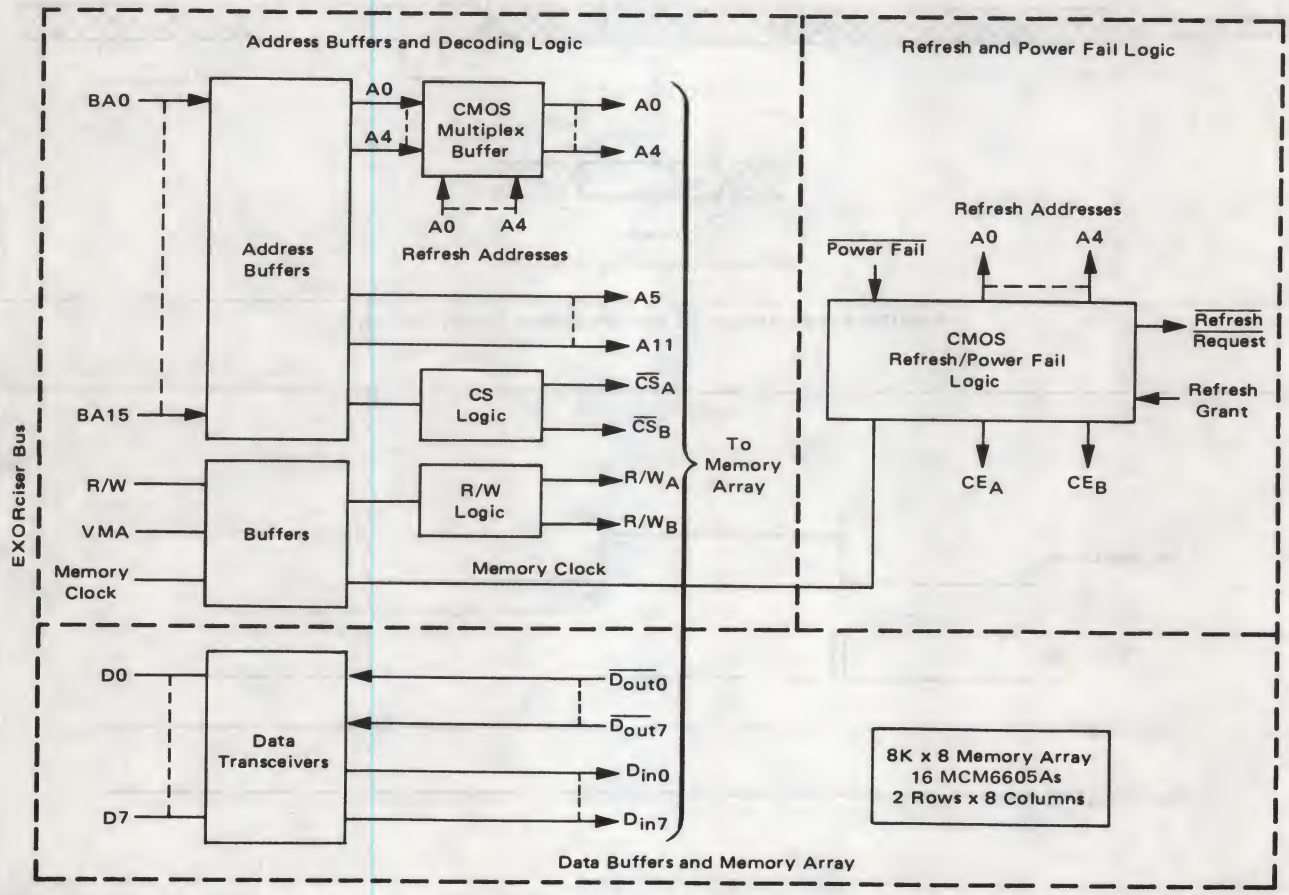

FIGURE 3 – Non-Volatile Memory System Block Diagram

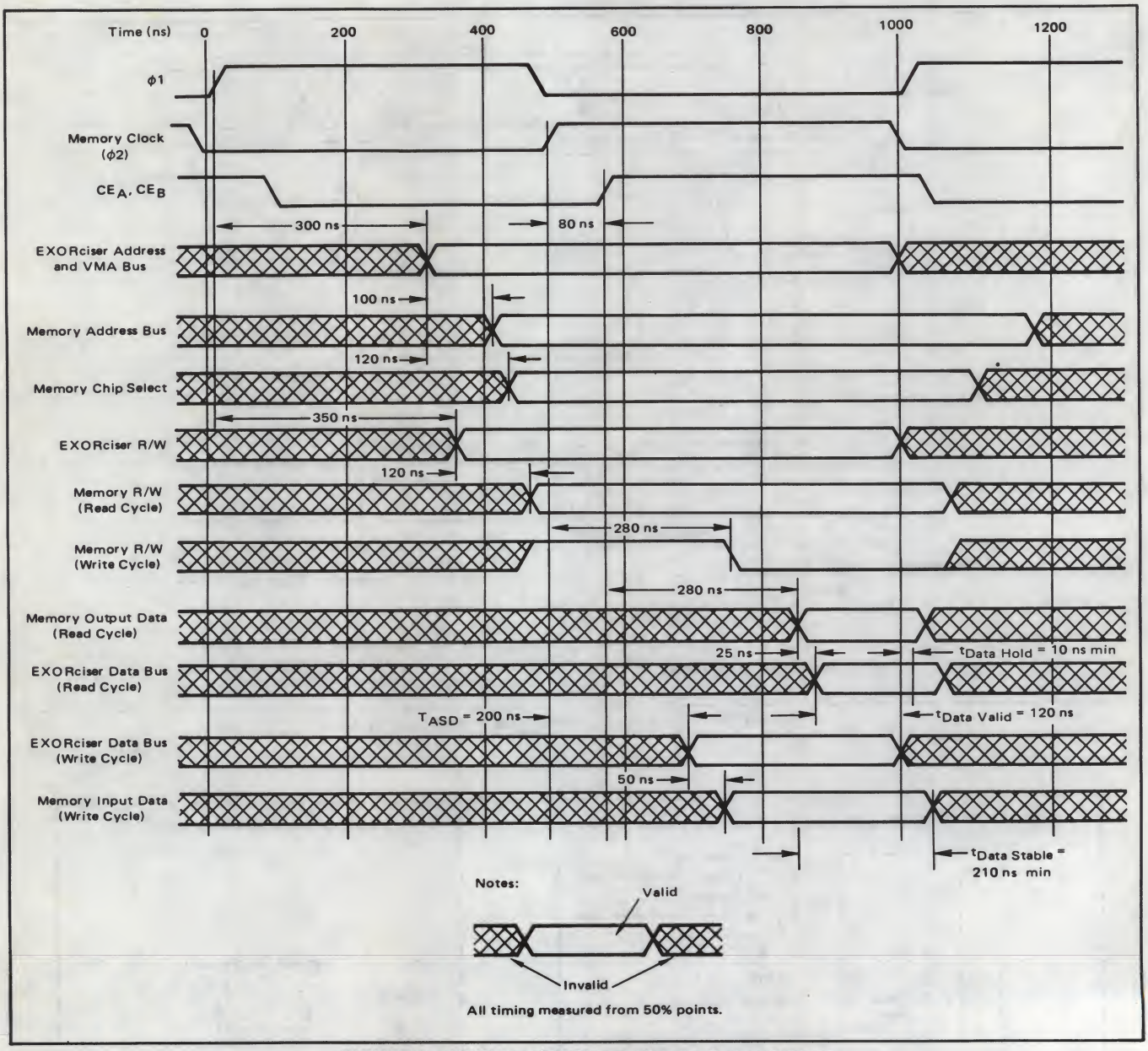

FIGURE 4 – EXORciser/4K Memory System Timing Diagram

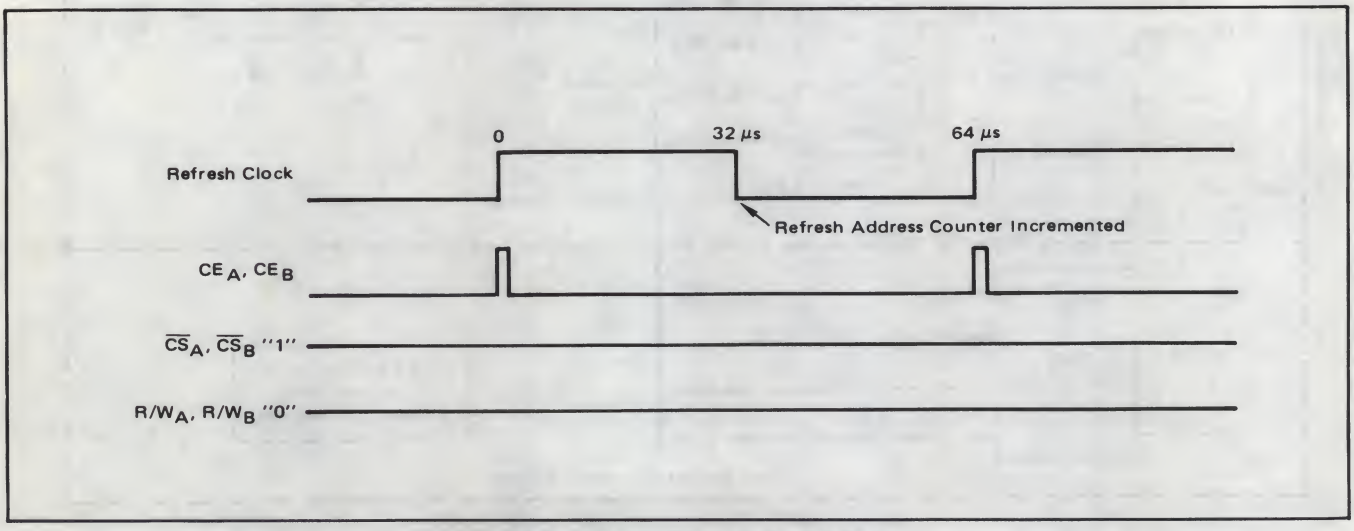

FIGURE 5 – Memory Timing in Standby Mode

ADDRESS BUFFERS AND DECODING

Figure 6 is a logic diagram of the address buffers, decoding logic and refresh address multiplexer. Address and data lines from the EXORciser are buffered from the capacitance of the memory array in order to provide a small load to the bus. This increases the EXORciser flexibility because it can easily be expanded. Since the addresses are valid on the EXORciser bus 300 ns into $\phi 1$, 200 ns is available to set up the address on the memories. The worst case input capacitance on the address lines of the MCM6605A is 5 pF/input. A system of 16 memory devices (8K bytes) presents a total capacitive load on the address lines of only 100 pF (20 pF stray capacitance). Since 200 ns is available to set up the addresses on the memory devices, no high current buffers are required to drive the memories. A0 through A4 must be multiplexed with the refresh addresses so that all 32 columns will be refreshed every 2 ms. Because of the requirement of low current drain in the standby mode, an MC14503* CMOS buffer with a three-state output is used to meet the multiplexing requirement. The buffers have sufficient current drive capability to drive the address line capacitance within 100 ns. An open collector TTL gate is used to translate to +12 V CMOS levels. A0 through A11 are driven with Ground and 12 V logic levels so that +5 V is not required in the standby mode. A5 through A11 are clamped to Ground during a refresh cycle so that they will remain stable.

The high order address lines (A12 through A15) are used to decode one 4K block of memory out of the 16 total possible blocks in the 65K address map. The addresses and their complements are routed through hexadecimal switches to MC7430 NAND gates in order to create a $\overline{CS}$ signal for each 4K byte of memory. By rotating the hexadecimal switches (S3 and S4), all combinations of true and complement addresses can be routed to the NAND gates, thereby selecting one of the sixteen 4K blocks. VMA and $\overline{REF}_A$ are also inputs to these NAND gates: VMA is a Valid Memory Address signal on the bus indicating that the address lines are valid and $\overline{REF}_A$ is a control signal indicating that a refresh cycle is taking place. During a refresh cycle, $\overline{REF}_A$ goes low forcing $\overline{CS}_A$ and $\overline{CS}_B$ high (a refresh cycle for the memory devices is a write cycle with the $\overline{\text{Chip Select}}$ held high). The output of the MC7430 is translated to 12-V CMOS levels with the open collector gates and buffered with the MC14503 three-state buffer. The capacitive loading on each set of three paralleled drivers is 60 pF, allowing $\overline{\text{Chip Select}}$ to be decoded and valid 120 ns after addresses are valid on the data bus. During the standby mode (Bat = "1") the CMOS buffer is disabled allowing the 3.3 k ohm resistors to pull $\overline{CS}_A$ and $\overline{CS}_B$ high for continuous refreshing.

The Read/Write signal is received by an MC8T26** and then decoded in the following manner: A write inhibit feature is provided using switches S1 and S2 for each 4K byte block of memory so that in a ROM simultation application the memory can be protected from extraneous write operations due to programming or operator errors. The Ready-Modify-Write cycle of the MCM6605A is used in this application because it requires a shorter data valid time ($t_{\text{Data Stable}}$) than a normal write cycle (see Figures 2b and 2c). This feature is desirable because the EXORciser places valid data on the bus for the last 300 ns of a Write cycle. In order to delay the write pulse to the memory array until the data is valid on the Data Inputs of the memory array, a write inhibit pulse is combined with the EXORciser R/W signal in the MC7420 NAND gates. This write inhibit pulse is generated by the MC8602 monostable multivibrator triggered from the leading edge of the Memory Clock bus signal. The effect of this added delay can be seen from Figure 4 when comparing the memory array R/W line for a read and a write cycle. Note that for a write cycle, the R/W of the memory array is inhibited from dropping to the Write mode until memory input data is valid.

The refresh control signal ($\overline{REF}_A$) is combined with the output of the MC7420 in an MC7408 AND gate in order to force a write signal on the memory R/W lines while in a refresh cycle. Translation and buffering is accomplished in a similar manner as with the Chip Select signals. When in the standby mode (Bat = "1") the MC14503 buffers are disabled allowing the 3.3 k resistor to establish a zero level on the R/W line of the memory array for continuous refreshing.

DATA BUFFERS AND MEMORY ARRAY

The EXORciser data bus is bidirectional, while the MCM6605A memory has separate data inputs and outputs. The MC8T26 data bus receiver/driver buffers the capacitance of the memory array (very low, about 30 pF per data line) and combines the Data Input and $\overline{\text{Data Output}}$ of the memory array into one bidirectional bus as shown in Figure 7. The $\overline{\text{Data Out}}$ of the memory devices is inverted from the Data In, requiring an extra inverter (MC7404) in the data path when working with a non-inverting bus (i.e., the data is returned to the bus in the same sense it was received).

During a memory write cycle, the data is valid on the data bus 200 ns (T_{ASD}) after the leading edge of the Memory Clock. With a 50 ns delay through the bus translators, the data setup requirement of the memories (210 ns) is easily met (see Figure 4). A memory read cycle requires a data setup time on the data bus of 120 ns. The access time of the memory from the leading edge of the CE signal plus the bus transceiver delay is 305 ns, which is compatible with the setup time required.

REFRESH AND CONTROL LOGIC

The refresh control logic shown in Figure 8 handles the refreshing of the memory during both operating and standby modes. The timing is shown in Figure 9.

The refresh timing is controlled by an astable multivibrator constructed with an MC3302 comparator. This

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* MC14503 to be introduced-replacement for MM80C97.
**MC8T26 to be introduced-replacement for N8T26.

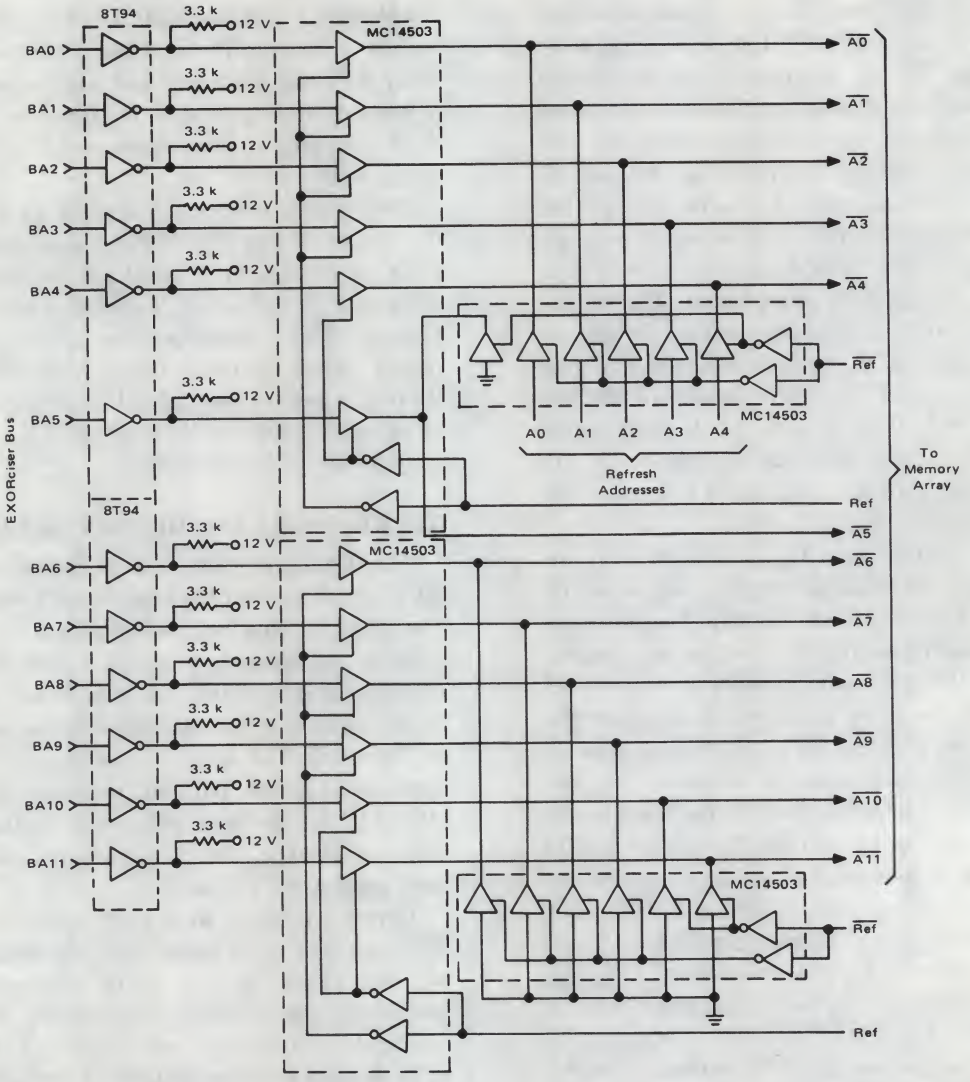

FIGURE 6 – Address Buffers and Decoding Logic

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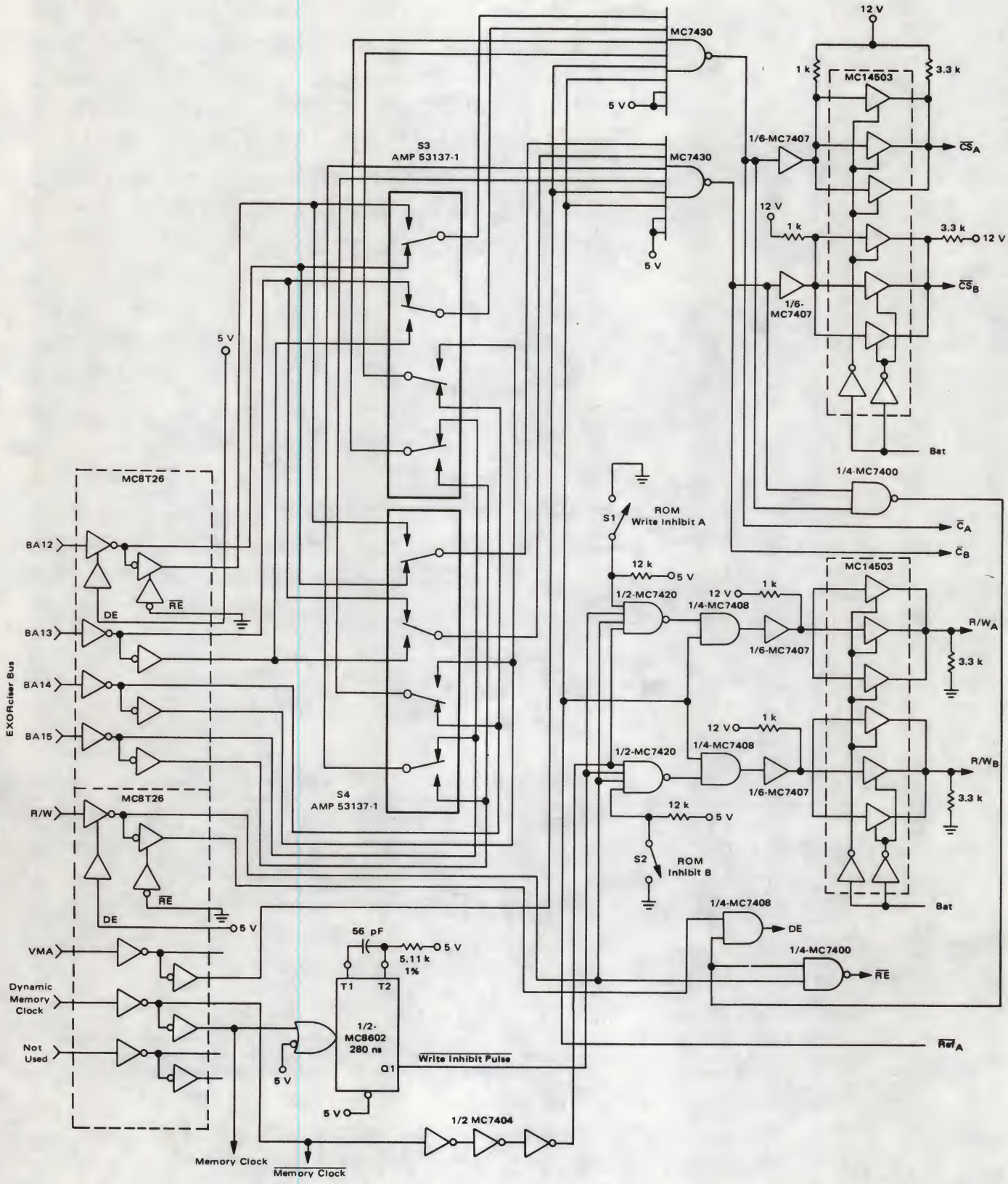

FIGURE 6 – Address Buffers and Decoding Logic
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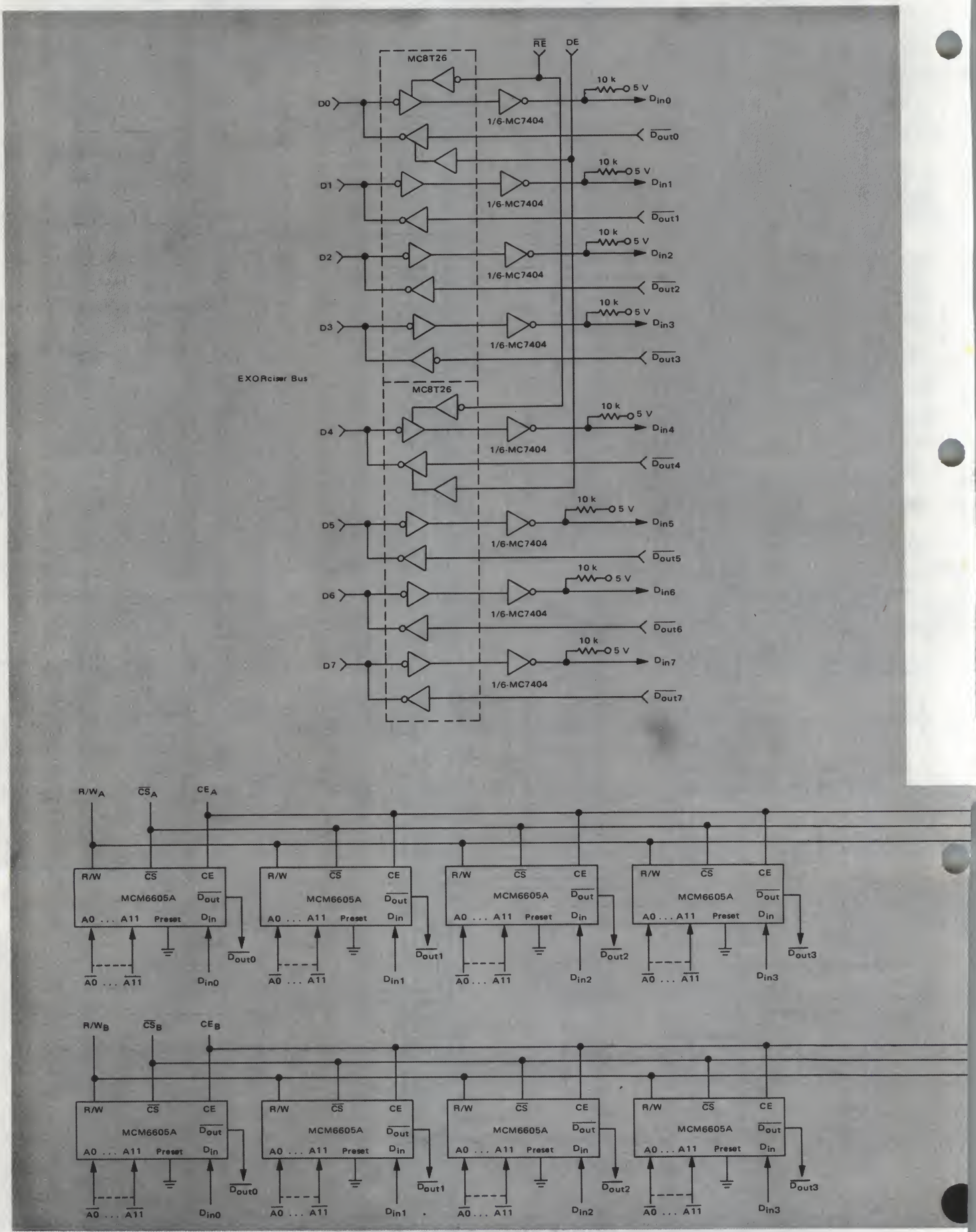


FIGURE 7 – Data Buffers and Memory Array

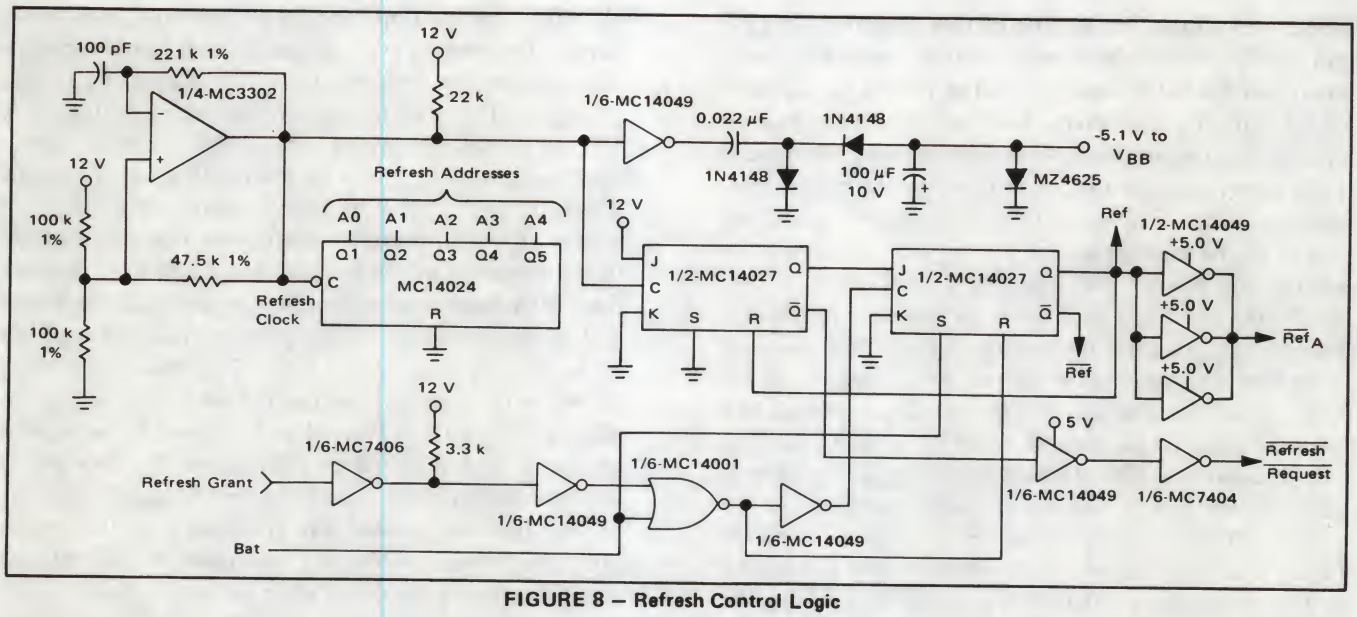


FIGURE 8 – Refresh Control Logic

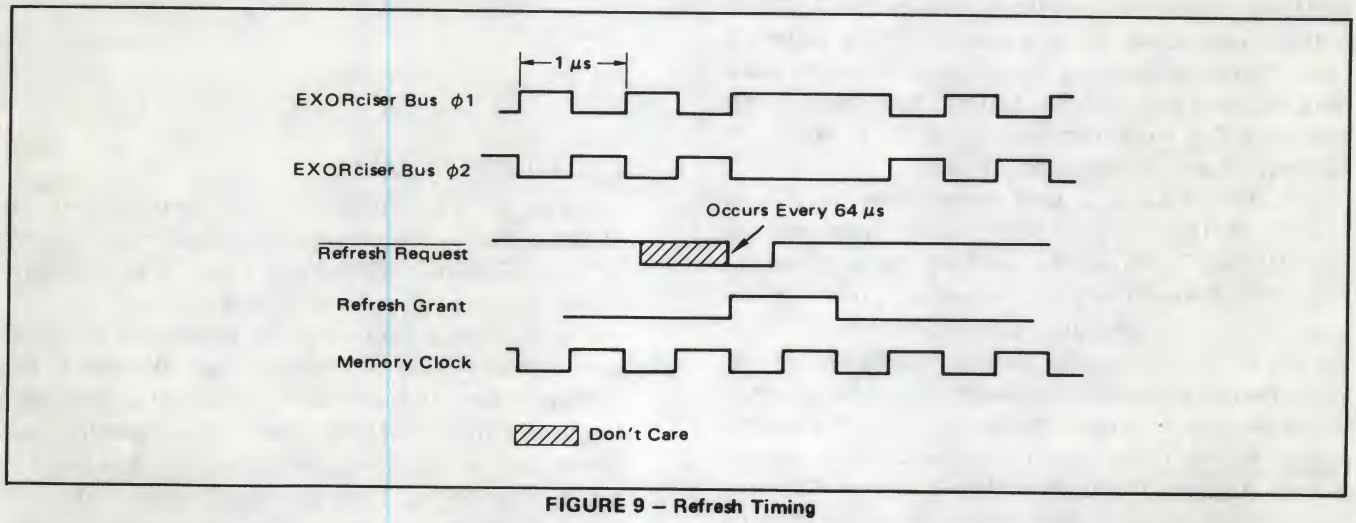
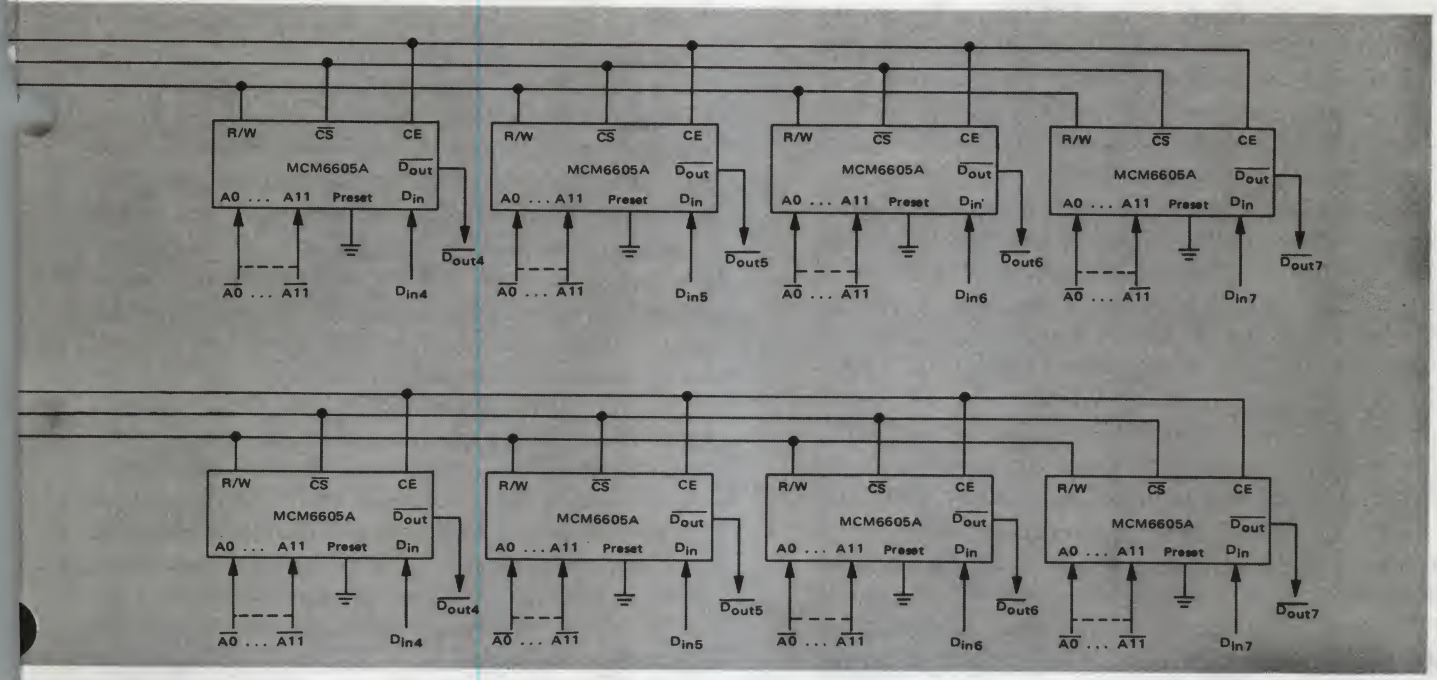


FIGURE 9 – Refresh Timing



device was chosen for its low current consumption (1.5 mA max) and single supply voltage operation, both important for battery operation. The refresh requirement of 32 refresh cycles every 2 ms is handled by stealing cycles from the processor. This cycle stealing results in a 1.6% slower program execution rate than the basic microprocessor clock frequency. During the refresh cycle, the clocks to the microprocessor are "stretched" during the $\phi 1$ high and the $\phi 2$ low times by 1 μs as shown in Figure 9. During this 1 μs period, the memory executes a refresh cycle. In order to minimize the effects of memory refresh on microprocessor program execution, the 32 refresh cycles are distributed over the 2 ms period, one occuring every 64 μs. Refresh could be done in a burst of 32 cycles every 2 ms but this would cause a larger gap in program execution, which in this case was undesirable.

The MC3302 produces the 64 μs signal shown in Figure 5 to time the refresh requirement, and also is used in the generation of the -5 V supply required by the MCM6605 memory. Since these functions are required in the standby mode, which is powered by the battery, a CMOS buffer is used in a charge pump circuit to minimize current drain from the battery. This charge pump creates -5 V at 3 mA from the 12-V battery to satisfy the bias requirements of the memory devices.

The Refresh Clock is used to increment the address counter (MC14024) and to clock the refresh handshaking logic (MC14027). $\overline{\text{Refresh Request}}$ goes low on the leading edge of the Refresh Clock, thus requesting a refresh cycle. Logic in the clock generation circuitry stretches the high portion of $\phi 1$ and the low portion of $\phi 2$ while sending back a Refresh Grant signal. This stretching of the $\phi 1$ signal delays program execution during this cycle. The leading edge of Refresh Grant starts the refresh cycle and cancels $\overline{\text{Refresh Request}}$. The trailing edge of Refresh Grant returns the refresh logic to the normal state and the memory is ready for a memory access. The trailing edge of the Refresh Clock then increments the refresh address counter in preparation for the next refresh cycle.

Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal is shown in Figure 10, with the timing given in Figure 11.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the Memory Clock by use of the three-state feature of the MC14503. The Memory Clock (used during normal operation) is translated to 12-V levels by use of an MC3460 clock driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory band addressed) to conserve power is accomplished by internal logic within the MC3460.

Since the $\overline{\text{Power Fail}}$ signal will occur asynchronously with both the $\overline{\text{Memory Clock}}$ and the refreshing operation (Refresh Clock), it is necessary to synchronize the $\overline{\text{Power Fail}}$ signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to direct set half of the MC14027 flip-flop, the output of which, Ⓑ, then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the Power $\overline{\text{Fail}}$ signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of Power Fail and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with Memory Clock. The outputs of this flip-flop, labeled Bat and $\overline{\text{Bat}}$, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1".

SYSTEM PERFORMANCE

Figure 12 is a photograph of the breadboard of this dynamic memory system. This breadboard was interfaced with an EXORciser system and tested using a comprehensive memory test program written in-house.

Figure 13 is a photograph of waveshapes associated with alternate reads and writes in one 4K bank of the memory system. Included also is the M6800 program used to generate these waveforms. This type of operation produces repetitive signals on the memory board in order to aid troubleshooting. Note the refresh cycle sandwiched in among the read and write cycles, and that the decoding of the CE signals produces no clocks on CE_A (accesses are to bank B), except during refresh.

Figure 14 shows the printed circuit memory array used to interconnect the memories. The addresses are bussed between the 4K memory chips in the horizontal direction. Data lines are bussed in the vertical direction. The MCM6605 4K RAM has power and ground pins on the corners of the package allowing wide, low impedance power and ground interconnects within the memory array. Decoupling capacitors were used as follows within the memory array: +12 V - one 0.1 μF ceramic per package, +5 V - one 0.01 μF ceramic for every three packages, and -5 V - one 0.01 μF ceramic for every three packages. Figure 15 is a photograph showing the ripple on the power supplies caused by accesses to one 4K byte bank of memory as shown in the photograph. The +12 V line supplies the most current to the array and is the one on which the most care in decoupling (wide PC lines and distributed capacitance) should be taken. Placement of the V_{DD} pin on the corner of the package allows the designer the option to do this easily.

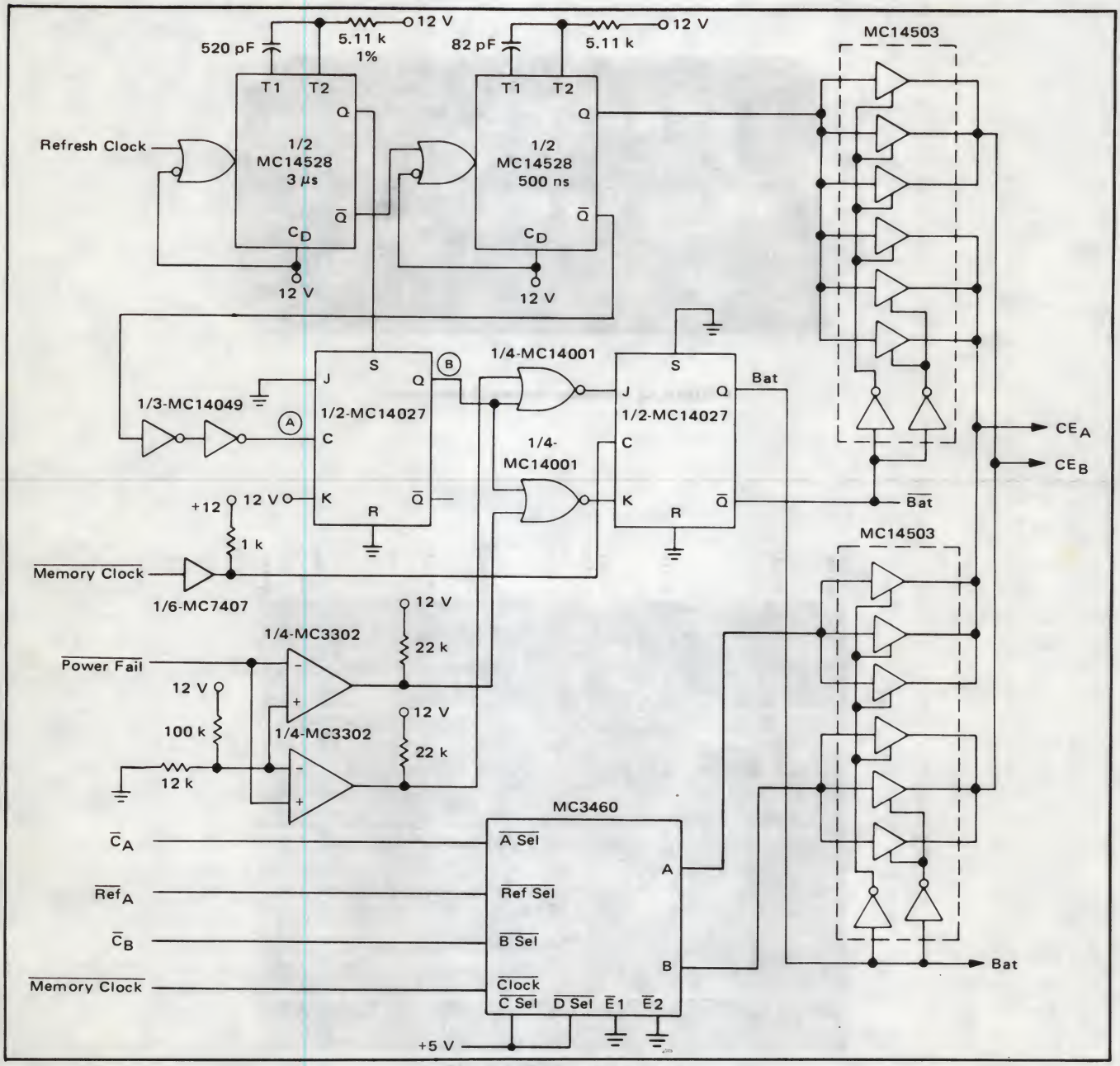


FIGURE 10 – Power Fail Logic

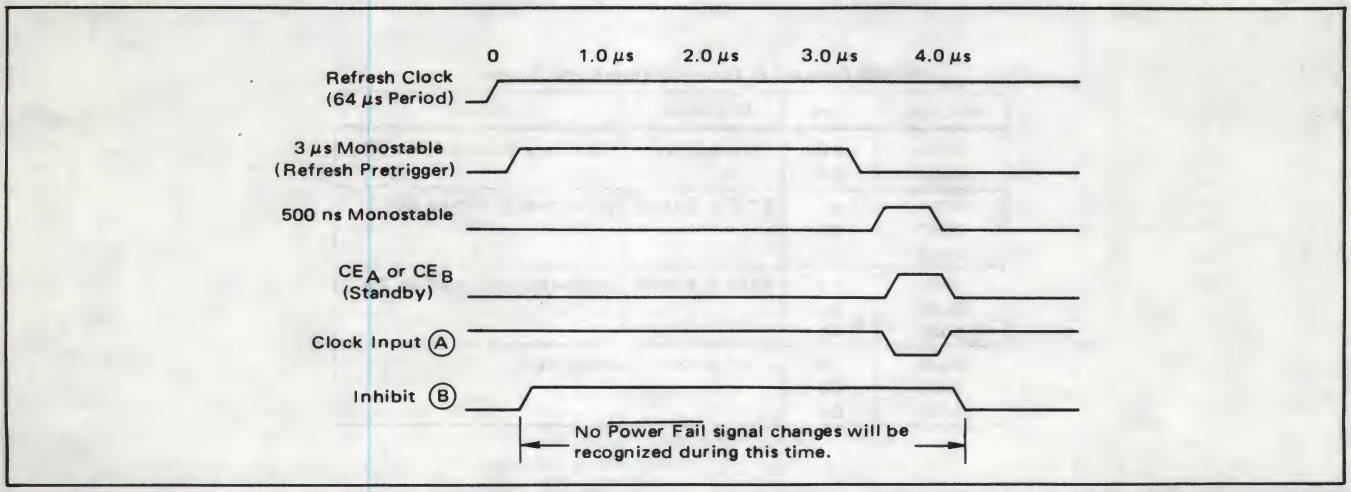


FIGURE 11 – Power Up/Down Synchronization

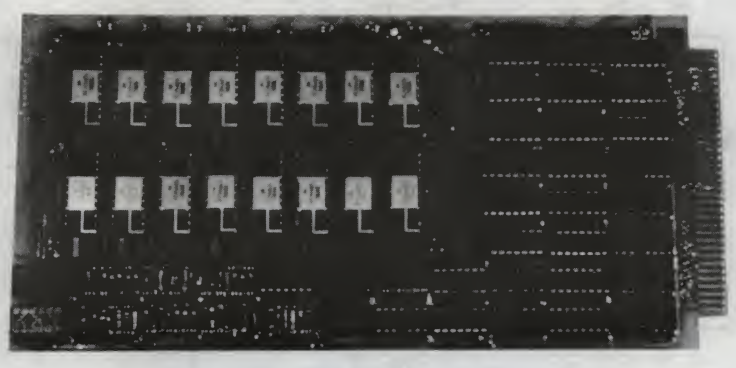
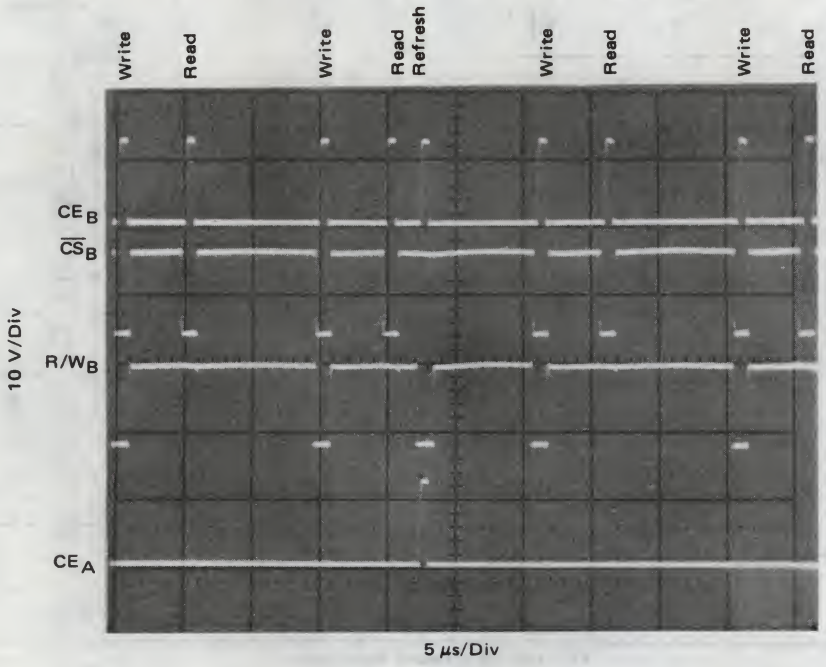


FIGURE 12 – Memory System Breadboard



M6800 Program to Generate Waveforms Shown

Address	Data	Mnemonic	Comment
0000 0001	B6 55	LDA #$55	Load data to be written (55)
0002 0003 0004	B7 30 00	STA A $3000	Store data in address 3000
0005 0006 0007	F6 30 00	LDA B $3000	Read data from address 3000
0008 0009 000A	7E 00 02	JMP $0002	Loop back

FIGURE 13 – Alternate Read and Write Memory Accesses

TABLE 3 – Battery Characteristics

Battery	Ampere-Hours	Size (L x W x H)	Weight	Support Time*
Globe GC 12200	20	6.9" x 6.5" x 4.9"	16.75 lbs.	35 days (850 hrs)
Globe GC 1245-1	4.5	6" x 2.5" x 4"	4.5 lbs	8 days (192 hrs)
Globe GC 1215-1	1.5	7" x 1.3" x 2.6"	1.5 lbs	2.6 days (63.75 hrs)
Burgess MP 202	0.6	3.4" x 1.4" x 2.3"	11.6 oz	1.25 days (30 hrs)
Burgess 12.0 V 225 Bh	0.225	3.5" H x 1" Diam.	4.65 oz	0.47 day (11.25 hrs)

*Assumes 20 mA average current drain (14 mA for memory and 6 mA for power fail detection circuitry) and a battery voltage range during discharge from 13 to 11 V.

SUMMARY

This application note has described the design of an 8K byte memory system, based on the MCM6605A 4K x 1 dynamic RAM, to provide non-volatile operation with a minimum of standby current. Tests on the breadboard memory system indicate standby currents typically 14 mA from a 12 V battery. The discussion has shown that a dynamic memory refresh requirement can be handled with minimal control logic. For memory sizes in the area of 8K bytes, the higher bit density of the 4K chip makes the system design cost effective when compared to an equivalent static memory design. In the area of non-volatility, the standby mode inherent in a dynamic memory makes it a "hands down" winner when compared to a static memory design of this size.

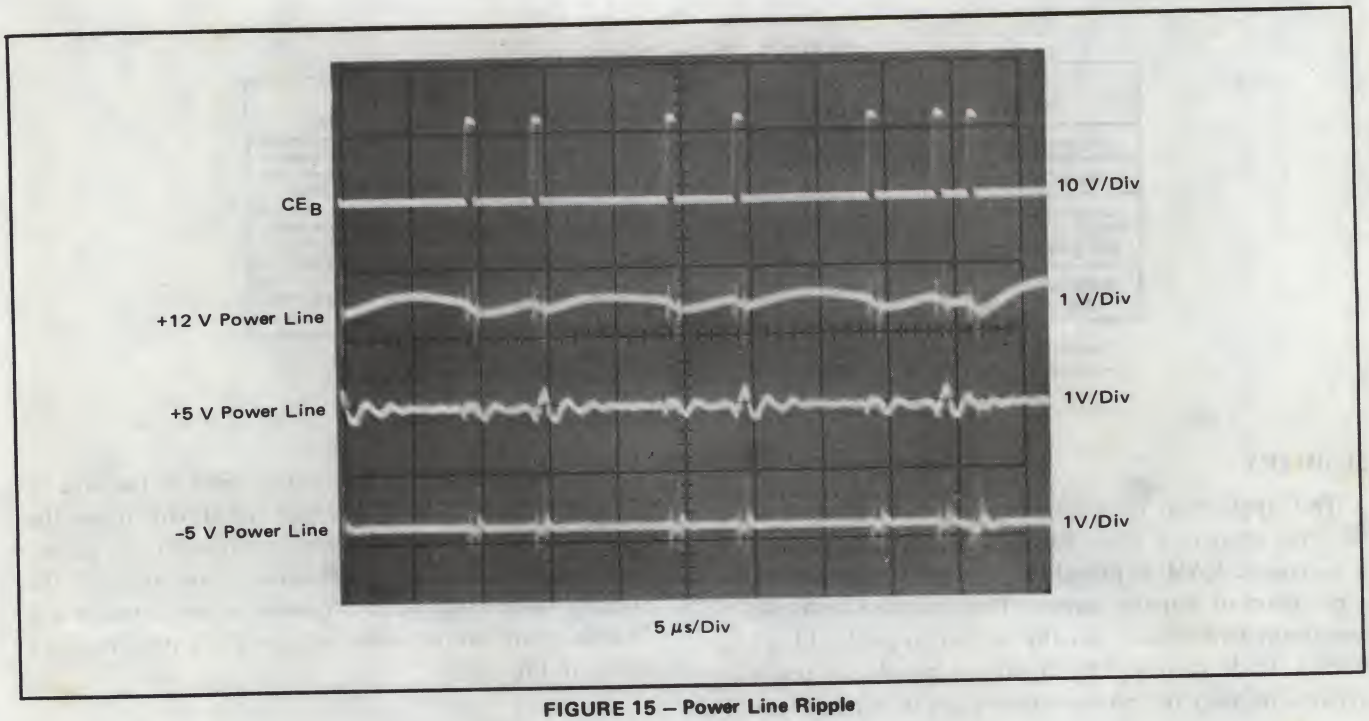


FIGURE 15 – Power Line Ripple

The dc power dissipation of this memory system is shown in Table 1. Of these current drains, the most critical to non-volatile operation is the current requirement in the standby mode in which the current would probably be supplied from a battery. A breakdown of the typical current required from +12 V to maintain the memory in the standby mode is shown in Table 2.

By using CMOS for the refresh logic and capacitance drivers, a dynamic memory, and a low current refresh oscillator, the standby current has been reduced to a level that can be supplied easily by a battery. Table 3 is a brief list of various capacity 12-V batteries that could be used to power a system of this type in the standby mode. Support time runs from one-half to 35 days and can be made as long as desired if sufficient battery capacity is available.

TABLE 1 – 8K x 8 Non-Volatile Memory System Power Requirements (1-MHz EXORciser Clock Rate)

Mode	Power Supply	Current	
		Typical	Maximum
Operating	+12 V*	100 mA	300 mA
	+5 V	600 mA	860 mA
Standby	+12 V	14 mA	20 mA
	+5 V	No +5 V Supply required	

*Because memory is dynamic, the +12 V current requirement is dependent on rate of memory access.

TABLE 2 – Standby Mode Current Allocation

Circuit Section	Typical Current
+12 V Current (V_{DD})	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

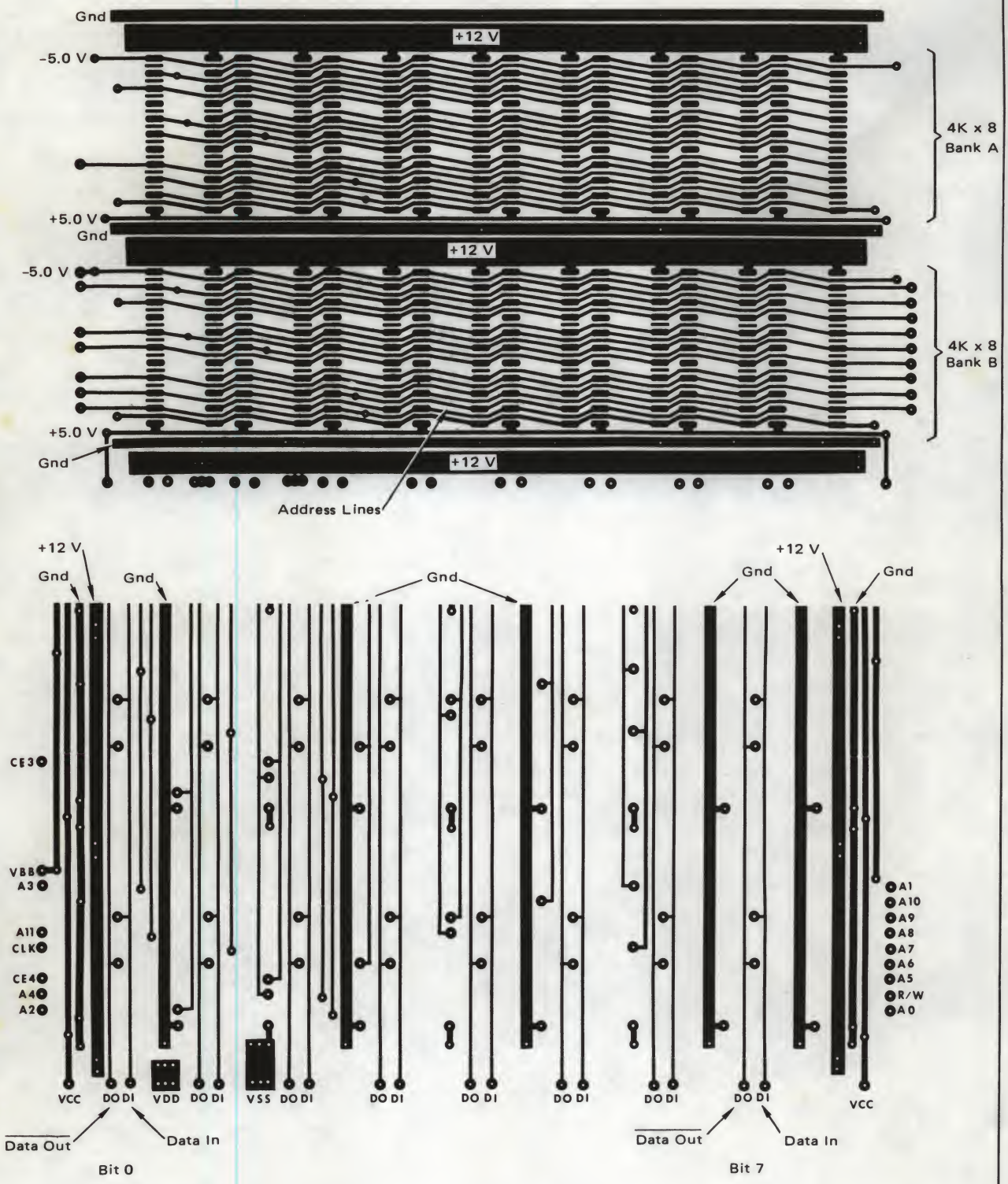


FIGURE 14 – Memory PC Board Array

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